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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,011	05/14/2001	Martin J. Ratcliffe	00-323 1496.00121	1191

7590 02/27/2004

Intellectual Property Law Department
LSI Logic Corporation
M/S D-106
1551 McCarthy Boulevard
Milpitas, CA 95035

EXAMINER	
ROSARIO-VASQUEZ, DENNIS	
ART UNIT	**PAPER NUMBER**
2621	

DATE MAILED: 02/27/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,011	RATCLIFFE, MARTIN J.	
	Examiner	Art Unit	
	Dennis Rosario-Vasquez	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *May 14, 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *May 14, 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Applicant's claim for domestic priority under 35 U.S.C. 120 is acknowledged.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-8, 11-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Malinowski et al. (US Patent 5,574,572 A).

Regarding claim 15, which is representative of claims 1,16, Malinowski et al. discloses an apparatus (Fig. 6) for variably scaling video picture signals ("Color video images may be scaled" at Malinowski et al. col. 6, line 58 and figure 1, labels "Y" and "U,V") comprising:

means for (fig. 6, numerals 52 and 54 located on the left side of figure 6) generating one or more data signals vertically scaled to a first value ("order of vertical...scaling" at Makinowski et al. , col. 6 line 62) in response to (i) said video picture signals and (ii) one control signal (Makinowski et al. , fig. 2, label "K1" is a control signal or "upscaling factor K (Makinowski et al., col. 3, line 47)" of the interpolator as shown in figure 2. The control signal is located within the interpolator of fig.6, num. 52); and

means for (fig. 6, numerals 52 and 54) generating one or more output signals horizontally scaled to a second value ("order of... horizontal scaling" at Makinowski et al. , col. 6 line 62) in response to (i) said one or more data signals and (ii) said one or more control signals (Figure 6, numerals 52 and 54 on the right side of figure 6 have the same characteristics of numerals 52 and 54 located on the right side of figure 6), wherein said first value and said second value are independently selectable (Makinowski et al. states," the vertical and horizontal scaling factors may be independent (col. 7 lines 1,2).") .

Regarding claim 2, Makinowski et al. discloses the apparatus according to claim 1, wherein said first circuit comprises (i) a luma circuit configured to generate a luma component of said output signals (fig. 6, label "Y" is luminance component) and (ii) a chroma circuit configured to generate one or more chroma components of said output signals (fig. 6, label "U,V" is a chrominance signal). Makinowski et al. states," With reference to FIG. 6, color video input may be separated into Y and UV components and provided to staged interpolators 52 and filters 54...(col. 6 lines 59-62).") Therefore either interpolator 52 or filter 54 can function as a luma circuit or chroma circuit.

Regarding claim 3, which is representative of claim 17, Makinowski et al. discloses the apparatus and method according to claims 1 and 16, wherein said second circuit is further configured to decimate (fig. 6, num. 54 or fig. 4 and fig. 5, numeral 40 are like parts at col. 6, lines 32 and 66) on the right side of figure 6 is a decimator and interpolate (fig. 6, num. 52 is an interpolator on the right side of figure 6) said data signals.

Regarding claim 4, which is representative of 19, Makinowski et al. discloses the Apparatus according to claims 1 and 16, wherein said apparatus is programmable ("process of positioning the U and V outputs" using hardware at col. line. 8 ,lines 10,11) to scale said output signals to one or more display modes. Multiple display formats (4:2:2 and 4:2:0 output formats) are disclosed at col. 8 lines 35-38)

Regarding claim 6, Makinowski et al. discloses the apparatus according to claim 4, wherein said one or more display modes are in a range of 0.25 times to 4.0 times said video picture signals. Makinowski et al. states," For downscaling, the input pixel stream is initially upscaled by an upscaling factor of between one and two chosen so that the result can be subsequently downscaled by a power of two to provide the desired final scaling (col. line. 6, lines 25-28)." Therefore if the scaling factor was selected to be .50 then a final scaling of .25 is achieved. On the otherhand, Makinowski et al. states," Upscaling is a special case in which there is no decimation and in which the upscaling factor is not limited (col. line. 6, lines 32-34)."

Regarding claim 7, Makinowski et al. discloses the apparatus according to claim 2, wherein said luma circuit comprises:

a first memory circuit configured to buffer (Figure 2, num. 22 and fig. 4, num. 44 are buffers located within figure 6, numerals 52 and 54, respectively.) said video picture signals;

a first filter circuit (fig. 6, numerals 52 and 54 on the left side of figure 6) serially coupled to said first memory circuit (As shown in figure 2, num. 22) and configured to generate said luma component (The upper section above the dashed line of figure 6 in

the luma processing section);

and a second memory circuit serially coupled to said first filter circuit (fig. 6, numeral 52 on the right side of figure 6 includes a buffer 22 of figure 2) and configured to buffer said data signals.

Claim 8 is similar to claim 7, except for requiring a chroma circuit.

Regarding claim 8, Makinowski et al. discloses the apparatus according to claim 7, wherein said chroma circuit (Figure 6 depicts a chroma circuit with a dashed line that divides figure 6 into the chroma portion located under the dashed line. The upper half of figure 6 is the luma circuit which is similar in structure to the chroma circuit).

Regarding claim 11, Makinowski et al. discloses the apparatus according to claim 8, wherein said first filter circuit further comprises a first accumulator circuit configured to define a number ("accumulator that adds the number of increments across the image" at col. 3 lines 66,67) of said video picture signals to be buffered in said first memory circuit in response to said one or more control signals.

Claim 12 is similar to claim 11, except for requiring another similar set of components which was addressed in claim 8.

Regarding 13, which is representative of claim 18, Makinowski et al. discloses the apparatus and method according to claims 1 and 16, wherein said second circuit controls an output rate (A phase offset is used to position chroma and luma components at the output at col. line. 8, lines 10-13) of said data signals from said first circuit in response to said first value and said second value.

Claim 14 is similar to and addressed in claim 12 above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Malinowski et al. (US Patent 5,574,572 A) and in view of Chen et al. (US Patent 6,356,315 B1).

Regarding claim 9, Malinowski et al. teaches the apparatus according to claim 1, wherein said first circuit comprises said control signals that are "responsive to a predetermined upscaling factor K (Makinowski et al., col. 3 line 47)." in response to a microcontroller circuit ("accumulator" at Makinowski et al., col. 3, line 66).

Makinowski et al. does not teach the generator circuit of claim 9. However, Chen et al. does teach the generator circuit, wherein said generator circuit (Chen et al., fig. 1, num. 21:LUMINANCE DDA or CHROMINANCE DDA) is configured to generate said control signals ("SHIFT CONTROL", fig. 1, Chen et al.). Chen et al. states, " The DDA is programmed with the desired magnification/reduction ratio and provides signals that control shifting of input samples into the FIR filter and selection of FIR coefficients for the FIR filter (Chen et al. at col. line. 2, lines 31-35)."

It would have been obvious at the time the invention was made to one of ordinary skill in the art to use Chen et al.'s DDA as a controller to select Makinowski et al. control signals of fig. 2, "K1" because Chen et al.'s DDA ensures a proper sampling rate of

input data (Chen et al. , col. line. 2, line 33).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Makinowski et al. (US Patent 5,574,572 A) and in view of Chen et al. (US Patent 6,356,315 B1) and further in view of Fandrianto et al. (US Patent 5,982,459 A).

Regarding claim 10, Malinowski et al. teaches "scaling options available in a device incorporating the present invention that is used as a NTSC/PAL decoder...(col. 8, lines 40-42).", and accumulators at col. 3 line 66 for interpolation and col. 5 lines 1,2 for decimation).

Makinowski et al. does not teach the use of a single-chip MPEG-2 decoder as required of claim 10.

However, Fandrianto et al., in the field of endeavor of interpolation (col. 3 line. 18), does teach a single-chip (fig. 1, num. 110: VCP) MPEG-2 decoder (Fandrianto et al. at col. 3 lines 9-11).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to use Fandrianto et al.'s VCP single-chip with MPEG-2 decoding to modify Makinowski et al. accumulation calculations of interpolation and decimation because Fandrianto et al.'s VCP single-chip is capable of decoding multiple standard video formats MPEG 1 and MPEG 2 per a committee that propagates video standards (Fandrianto et al., col. line. 3, lines 11-15).

6. Claim 5 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malinowski et al. (US Patent 5,574,572 A) and in view of Iwase (US Patent 5,089,893 A).

Rgarding claim 20, which is representative of claim 5, Malinowski et al. teaches a display line when some of a picture is not displayed. Makinowski et al. states,"...for a given set of input pixels, interpolations are generated so long as the accumulation of dx does not increment beyond the next integer pixel value (col. 4 line 31-33)."

However, Makinowski et al. does not teach the remaining portions of claim 20.

Iwase, in the field of endeavor of scaling at col. 2 lines 37-41, does teach the remaining portion of claims 20 and 5 of automatically resetting a display line address ("address AD" at col. 4, lines 30,31).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to use the teaching of Iwase of automatically resetting an address line with Makinowski et al. teaching of not interpolating beyond the next integer pixel value because Iwase's resetting of an address line provides proper information for a "respective subfilter" (Iwase, col. 4 lines 25-47).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gadre et al. (US Patent 6,259,479 B1) is pertinent as teaching a method of decimating luminance and chrominance signals (fig. 4, numerals 92 and 96) using filters (fig. 4, num. 66).

Canfield et al. (US Patent 6,064,450 A) is pertinent as teaching a method of decimation (col. 6 lines 14-17) and interpolation or bi-directional prediction (col. line. 1, lines 14,15) using MPEG-2 (col. 1 lines. 4-7).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis Rosario-Vasquez whose telephone number is 703-305-5431. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DRV
Dennis Rosario-Vasquez
Unit 2621

LEO BOUDREAU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600